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Design for Testability and Performance of Arithmetic Logic Circuits

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***Abstract*- A set of test vectors that detects all single stuck-at faults on all primary inputs of a fan-out free combinational logic circuit will detect all single stuck –at faults in that circuit . A set of test vectors that detect all single stuck-at faults on all primary inputs and all fan-out branches of a combinational logic circuit will detect all single stuck-at faults in that circuit. Design of logic integrated circuits in CMOS technology is becoming more and more complex since VLSI is the interest of many electronic IC users and manufactures. A common problem to be solved by designers, manufactures and users is the testing of these Ics. Testing can be expressed by checking if the outputs of function systems (functional block, integrated circuits, printed circuit board or complete systems) correspond to the inputs applied to it. If the test of this function system is positive, then the system is good for use. If the outputs are different than expected. Then the system has a problem: so either the system is rejected (go/no go test), or a diagnosis is applied to it, in order to point out and probably eliminate the problem's causes.**

Keywords- CMOS, Testing, Fan out, IC, PCB, VLSI

I. INTRODUCTION

DSCH: Testing is applied to detect faults after several operations: design, manufacturing, packaging and during the active life of a system. Design for testability (DFT) is the ability of simplifying the test of any system. DFT could be synthesized by a set of techniques and design guidelines where the goals are:

a. minimizing costs of system production
b. minimizing system test complexity: test generation and application
c. improving quality and reliability

In the production process cycle, a fault can occur at the chip level. If a test strategy is considered at the beginning of the design, then the fault could be detected rapidly, located and eliminated at a very low cost. When the faulty chip is soldered on a printed circuit board, the cost of fault remedy would be multiplied by ten. And this cost factors continues to apply until the system has been assembled and packaged and then sent to users.

II. SCOPE OF TESTING

2.1 Engineering Test

The engineering test is a diagnostic test which fault location, failure analysis and design and / or process debugging

2.2 Manufacturing test

Manufacturing test is a characterization test 1.)Performance characterization: parametric test 2.)Reliability characterization: bathtub curve (aging)

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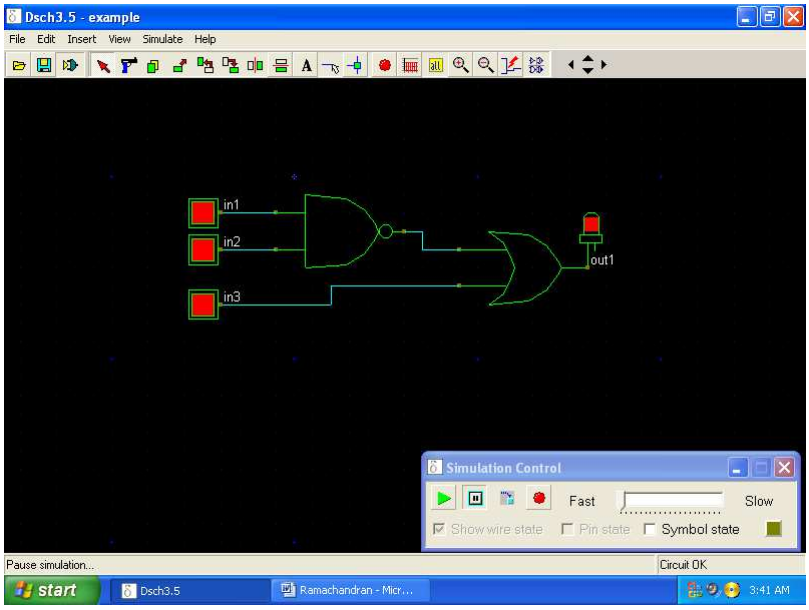
2.3 Production test

Simple parametric test, Functional test Reliability screening (burn-in)

3. Testing

Testing is a process which includes test pattern generation, test pattern application, and output evaluation

III. SIMULATION RESULTS



4.1 Arithmetic Logic Circuits

4.2.1 Truth Table: Generating the Reference Truth table

A	B	C(CORRECT)	C_f(a@0)	C_f(a@1)	C_f(b@0)	C_f(b@1)	C_f(c@0)	C_f(c@1)
0	0	0	0	0	0	0	0	1
0	1	0	0	1	0	0	0	1
1	0	0	0	0	0	1	0	1
1	1	1	0	1	0	1	0	1

4.2.2 Truth Table: Simulation of the fault free circuit & faulty circuits

A	B	C	Out Fault-free	Out A@0	Out A@1	Out B@0	Out B@1	Out C@0	Out C@1	Out X@0	Out X@1	Out S@0	Out S@1
0	0	0	1	1	1	1	1	1	1	0	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	1	0	1	1	0	1	1	1	1	0	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	1	1	1	1	1	0	1
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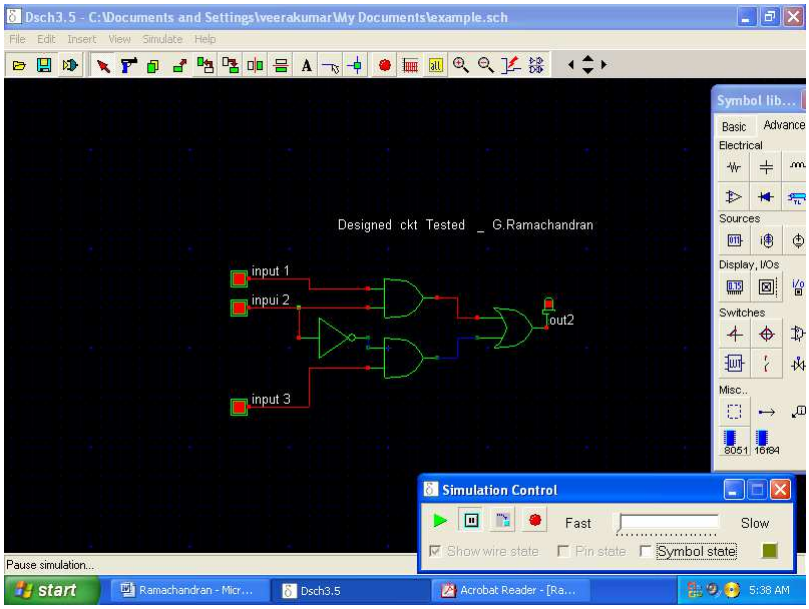
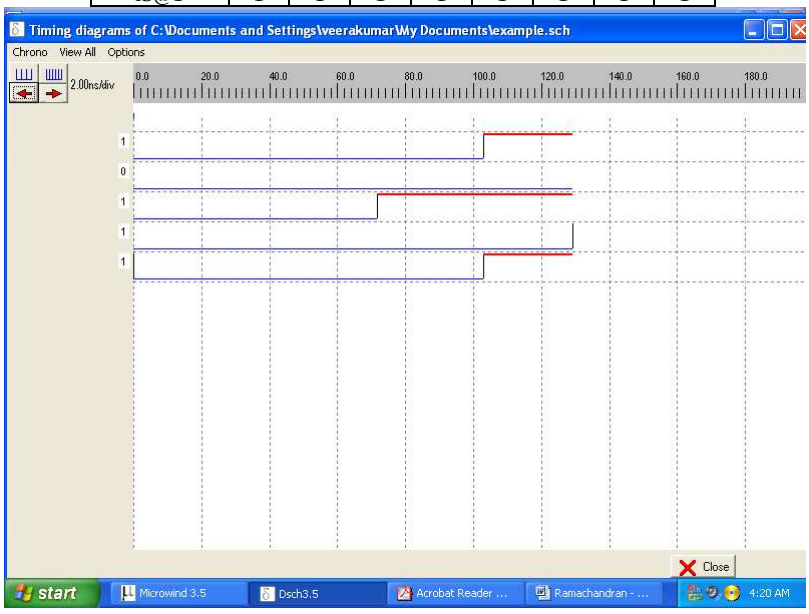


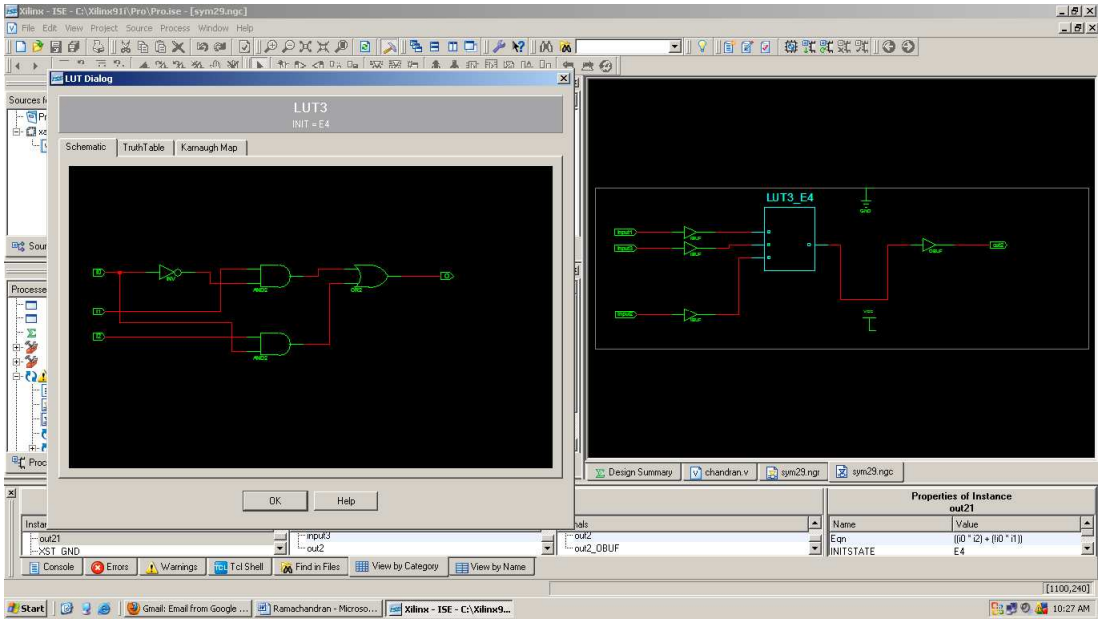
4.3 Arithmetic Logic Circuits- DSCH

4.4 Truth Table for faulty –free and faulty circuits

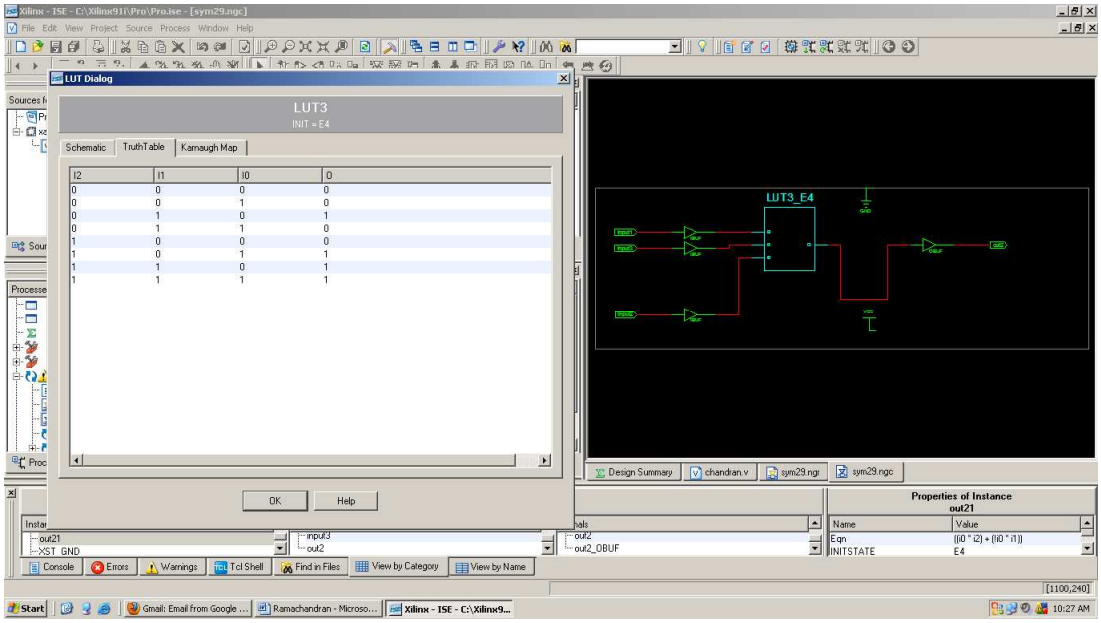
Time	000	001	010	011	100	101	110	111
Y(fault-free)	0	1	0	0	0	1	1	1
aS@0	0	1	0	0	0	1	0	0
aS@1	0	1	1	1	0	1	1	1
bS@0	0	1	0	1	0	1	0	1
bS@1	0	0	0	0	1	1	1	1
cS@0	0	0	0	0	0	0	1	1
cS@1	1	1	0	0	1	1	1	1
dS@0	0	1	0	0	0	1	1	0
dS@1	0	1	0	0	1	1	0	1
eS@0	0	1	0	1	0	1	1	1
eS@1	0	0	0	0	0	0	1	1
fS@0	0	0	0	0	0	0	1	1
fS@1	0	1	0	1	0	1	1	1
gS@0	0	1	0	0	0	1	0	0
gS@1	1	1	1	1	1	1	1	1
hS@0	0	0	0	0	0	0	1	1
hS@1	1	1	1	1	1	1	1	1
iS@0	0	0	0	0	0	0	0	0
iS@1	1	1	1	1	1	1	1	1



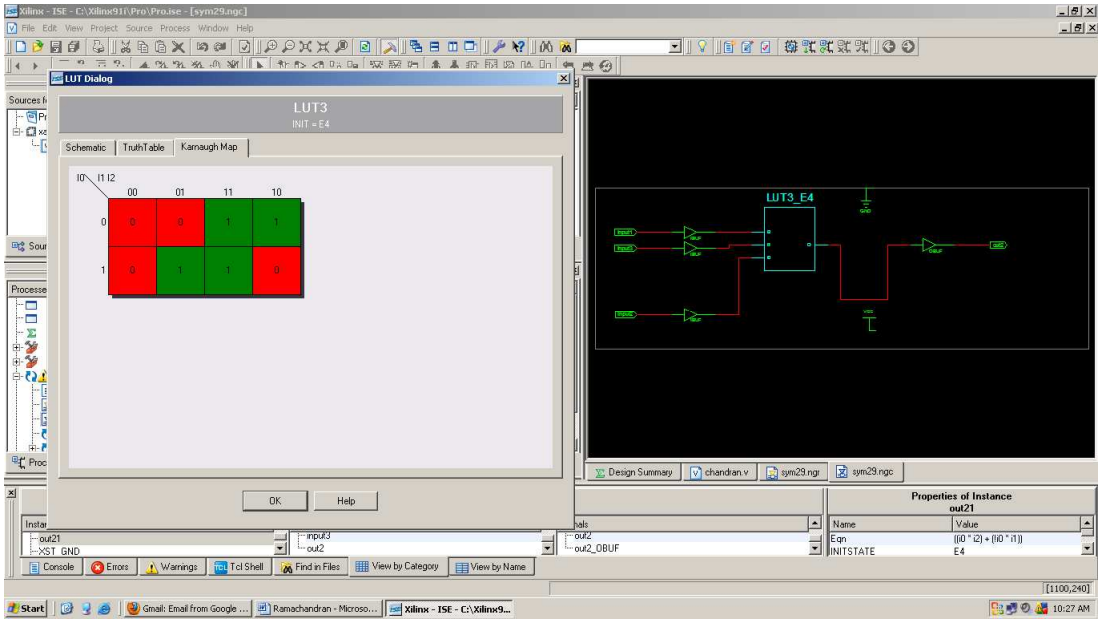
4.5 Timing wave form- DSCH



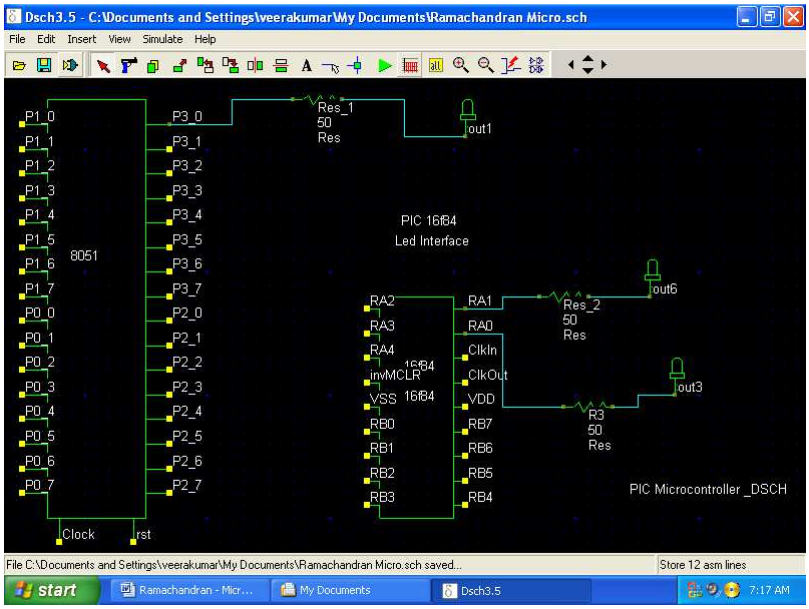
4.6 RTL Schematic circuits



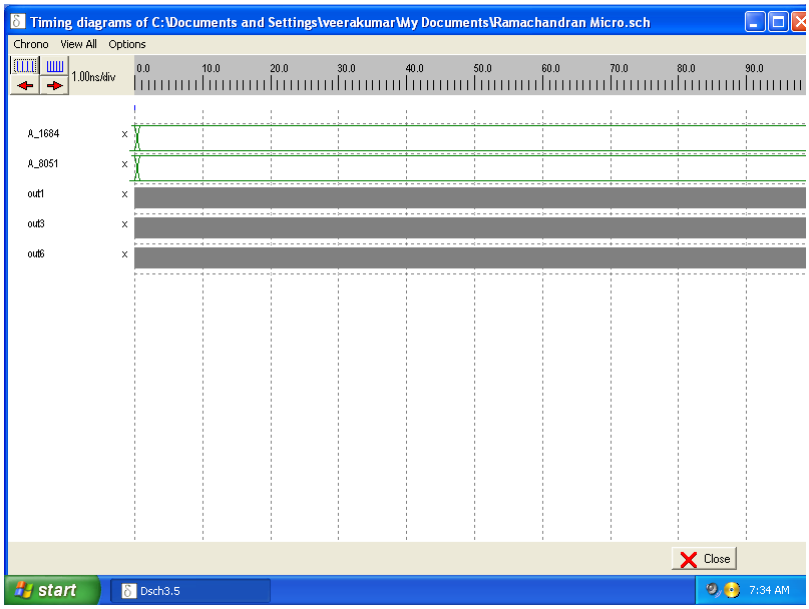
4.7 Truth Table & Schematic circuits



4.8 Implementation of K-Map& schematic circuits



4.9 Embedded systems 8051 &PIC 16F84A -DSCH



4.10 Timing Wave form- DSCH

IV. CONCLUSION AND FUTURE REFERENCE

The quality of a test set depends on its fault coverage (FC) as well as its size &FC (typically 98-99% single stuck faults) can be determined by fault simulation Stuck- at fault collapsing typically reduces the total number of faults by 50 to60%. Fault collapsing for stuck-at faults is based on the fact that a SAO at the input to an AND (NAND) gate is equivalent to the S@O (S@1) at the output of the gate. Similarly, a S@1 at the input to an OR (NOR) gate is equivalent to the S@1 (S@O) at the output of the gate. For an inverter, a S@0 (S@1) at the input is equivalent to the SA1 (S@0) at the output of the inverter. Furthermore, a stuck-at fault at the source (output of the driving gate) of a fan out –free net is equivalent to the same stuck-at fault at the destination (gate input being driven). Therefore, the number of collapsed stuck –at faults in any combinational circuit constructed from elementary logic gates (AND, OR, NAND, NOR, and inverter) is given by: Number of collapsed faults=2*(number of Pos +number of fanout stems) + total number of gate (including inverter) inputs-total number of inverters.

Test vector reduction consists to find the minimum set of test vectors which detect all single stuck –at faults.

REFERENCES

[1] G.Ramachandran, N.Manikanda Devarajan,T.MuthuManickam IJCER"Comparative Study and implementation Mixed Level&Mixed Signal Simulation using PSpice and VHDL"

[2] N. Weste, K. Eshraghian "Principles of CMOS VLSI design", Addison Wesley, ISBN 0-201-53376-6, 1993

[3] Liu] W. Liu "Mosfet Models for SPICE simulation including Bsim3v3 and BSIM4", Wiley & Sons, 2001, ISBN 0-471-39697-4

[4] Mohammed Ismail & Terri Fiez "Analog VLSI-Signal & Information Processing"1stEdition , Tata McGraw Hill Publishing company Ltd 2001.